PATENT
Docket No. 2207/8686

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Circuit and Method for Protecting 1-Hot and 2-Hot Vector Tags In a Cache In High Performance Microprocessors

the specification of which is attached hereto unless the following is entered:

was filed on	as United States Application Number or PCT International Application Number	and was amended on (if applicable)
December 29, 2000	09/750,094	

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

PRIOR FOREIGN APPLICATION(S)

I hereby claim foreign priority benefits under 35 USC §119(a-d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application(s) for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date (day/month/year)	Priority Not Claimed

PROVISIONAL APPLICATION(S)

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below:

Application Number		Filing Date	

PRIOR UNITED STATES APPLICATION(S)

I hereby claim the benefit under 35 USC §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 USC §112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

Application Number	Filing Date	Status (patented, pending, abandoned)

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

John C. Altmiller (Reg. No. 25,951); Shawn W. O'Dowd (Reg. No. 34,687); Robert L. Hails, Jr. (Reg. No. 39,702) of KENYON & KENYON with offices located at 1500 "K" Street NW, Suite 700, Washington, DC, 20005-1257, telephone (202) 220-4200, and at 333 W. San Carlos Street, Suite 600, San Jose, CA, 95110-2711, telephone (408) 975-7500;

and Alan K. Aldous (#31,905); R. Edward Brake (#37,784); Ben Burge (#42,372); Jeffrey S. Draeger (#41,000); Cynthia Thomas Faatz (#39,973); John N. Greaves (#40,362); Seth Z. Kalson (#40,670); David J. Kaplan (#41,105); Peter Lam (#44,855); Charles A. Mirho (#41,199); Leo V. Novakoski (#37,198); Thomas C. Reynolds (#32,488); Kenneth M. Seddon (#43,105); Mark Seeley (#32,299); Steven P. Skabrat (#36,279); Howard A. Skaist (#36,008); Gene I. Su (#45,140); Calvin E. Wells (#43,256); Raymond J. Werner (#34,752); Robert G. Winkle (#37,474); and Charles K. Young (#39,435) of INTEL CORPORATION.

PATENT
Docket No. 2207/8686

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

Direct telephone calls to:	**Send correspondence to:**
JOHN C. ALTMILLER (202) 220-4200	KENYON & KENYON 1500 K STREET, N.W., SUITE 700 Washington, D.C. 20005-1257

I hereby declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of first or sole inventor	Last Name **Quach**	First Name **Nhon**	Middle Name
Residence	City San Jose	State or Country California	Country of Citizenship USA
Post Office Address	Street 6522 Pfeiffer Ranch Road	City San Jose	State or Country & Zip Code California 95120
Signature ~~3/28/01~~ Nhon Quach N.Q.		Date N.Q. 3/28/01	

PATENT
Docket No. 2207/8686

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

Direct telephone calls to:	**Send correspondence to:**
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Full name of first or sole inventor	Last Name **Crawford**	First Name **John**	Middle Name
Residence	City Los Gatos	State or Country California	Country of Citizenship USA
Post Office Address	Street 15300 Winchester Blvd. #10	City Los Gatos	State or Country & Zip Code California 95030
Signature		Date	3·29·2007

PATENT
Docket No. 2207/8686

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

Direct telephone calls to:	**Send correspondence to:**
JOHN C. ALTMILLER (202) 220-4200	KENYON & KENYON 1500 K STREET, N.W., SUITE 700 Washington, D.C. 20005-1257

I hereby declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of first or sole inventor	Last Name **Mathews**	First Name **Greg**	Middle Name S.
Residence	City Santa Clara	State or Country California	Country of Citizenship USA
Post Office Address	Street 3655 Pruneridge Ave., Apt. 97	City Santa Clara	State or Country & Zip Code California 95051
Signature Gregory S Mathews		Date 3/28/01	

PATENT
Docket No. 2207/8686

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

Direct telephone calls to:	**Send correspondence to:**
JOHN C. ALTMILLER (202) 220-4200	KENYON & KENYON 1500 K STREET, N.W., SUITE 700 Washington, D.C. 20005-1257

I hereby declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of first or sole Inventor	Last Name **Grochowski**	First Name **Edward**	Middle Name
Residence	City San Jose	State or Country California	Country of Citizenship USA
Post Office Address	Street 5565 Yale Drive	City San Jose	State or Country & Zip Code California 95118
Signature Edward F. Grochowski		Date 3-30-01	

PATENT
Docket No. 2207/8686

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

Direct telephone calls to:	**Send correspondence to:**
JOHN C. ALTMILLER (202) 220-4200	KENYON & KENYON 1500 K STREET, N.W., SUITE 700 Washington, D.C. 20005-1257

I hereby declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of first or sole inventor	Last Name **Kosaraju**	First Name **Chakravarthy**	Middle Name
Residence	City Sunnyvale	State or Country California	Country of Citizenship India
Post Office Address	Street 1083 Rembrandt Drive	City Sunnyvale	State or Country & Zip Code California 94087
Signature K.S.Chakravarthy		Date 3/28/2001	

PATENT
Docket No. 2207/8686

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors	:	QUACH, N.T., et al.
Serial No.	:	09/750,094
Filed	:	December 29, 2000
For	:	CIRCUIT AND METHOD FOR PROTECTING 1-HOT AND 2-HOT VECTOR TAGS IN HIGH PERFORMANCE MICROPROCESSORS
Group Art Unit	:	2186
Examiner	:	J. LANE

Commissioner of Patents
Washington D.C. 20231

DECLARATION PURSUANT TO 37 C.F.R. 1.131

We, Nhon T. Quach, John H. Crawford, Gregory S. Mathews, Edward Grochowski and Chakravarthy Kosaraju, hereby declare the following:

1. We are the joint inventors of the subject matter claimed in U.S. Patent Application Serial No. 09/750,094, filed December 29, 2000 and entitled "CIRCUIT AND METHOD FOR PROTECTING 1-HOT AND 2-HOT VECTOR TAGS IN HIGH PERFORMANCE MICROPROCESSORS."

2. The invention described and claimed in the present application was conceived prior to December 28, 2000. Evidence of this fact is shown in the invention disclosure form attached as Exhibit A hereto, which was prepared and submitted to our employer at the time of the disclosure, Intel Corporation, prior to December 28, 2000.

3. We exercised diligence in constructively reducing the claimed invention to practice from at least a time prior to December 28, 2000 continuously up to December 29, 2000, the date on which the above-cited non-provisional patent application was filed. During that time, we provided information to patent counsel for preparation of the application, and reviewed/revised drafts of the application that was filed on December 29, 2000.

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Respectfully submitted,

Dated: 11/5/2002

Nhon T. Quach
Nhon T. Quach

Dated: _____

_____
John H. Crawford

Dated: _____

_____
Gregory S. Mathews

Dated: _____

_____
Edward Grochowski

Dated: _____

_____
Chakravarthy Kosaraju

PATENT
Docket No. 2207/8686

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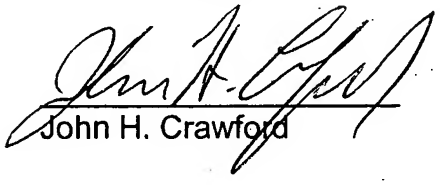
Respectfully submitted,

Dated: _____

_____
Nhon T. Quach

Dated: 11/14/2002


John H. Crawford

Dated: _____

_____
Gregory S. Mathews

Dated: _____

_____
Edward Grochowski

Dated: _____

_____
Chakravarthy Kosaraju

PATENT
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Respectfully submitted,

Dated: _____

_____
Nhon T. Quach

Dated: _____

_____
John H. Crawford

Dated: 11/8/02

Gregory S. Mathews
Gregory S. Mathews

Dated: _____

_____
Edward Grochowski

Dated: _____

_____
Chakravarthy Kosaraju

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Respectfully submitted,

Dated: _____

_____
Nhon T. Quach

Dated: _____

_____
John H. Crawford

Dated: _____

_____
Gregory S. Mathews

Dated: 11-20-02

Edward E Grochowski
Edward Grochowski

Dated: _____

_____
Chakravarthy Kosaraju

PATENT
Docket No. 2207/8686

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.	:	09/750,094
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Group Art Unit	:	2186
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Commissioner of Patents
Washington D.C. 20231

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Respectfully submitted,

Dated: _____

_____
Nhon T. Quach

Dated: _____

_____
John H. Crawford

Dated: _____

_____
Gregory S. Mathews

Dated: _____

_____
Edward Grochowski

Dated: 11/4/02

Chakravarthy Kosaraju

IDEA Invention Disclosure Form

13106 ARCHITECTURE/MPG COMM.

Complete and return to:
In D. Simon SC4-203 Department
or Hewlett-Packard: Intellectual Prop. Legal

Inventor(s)

Full Name: Nhon Quach Social Security No.: 586-14-9378
Residence Address: 6522 Pfeiffer Ranch Rd
Mailing Address:
Home Phone: (408) 268-6205 Work Phone: 765-6048 Mailstop: SC12-304
Employee No.: 10077866 Citizenship: U.S. Supervisor: Mulder, Hans
Employer: Intel Business Group: MPG Division/Lab: MPG

Signature: Date:
Please provide this same information — all of it — for each additional inventor, on additional pages as needed.

Invention

Title: Methods for protecting 1-hot vector tags in a cache in high performance microprocessors

Cluster: Unit: EAS/MAS/etc. Chap.:
Invent d as Part of: IAX P7 EM Merced EM H1 other (circle one)

Please attach a written description of the invention to this form. This information will be used by the IP Committee in det rmining whether to patent your invention, and by the patent attorney in learning the basics of your invention and in determining what other materials to study before meeting with you. This is your chance to educate the IP Committee members and "sell" your invention to them, and to get the patent attorney up the learning curve; so provide as much detail as you see fit. Please provide at least the following information:

1) the general purpose of the invention — what does it do? what problem does it solve?
2) the advantage of the invention over what others have done — how is it different or better than others?
3) the essential or basic elements of the invention — what is the invention? what are the key features?
4) the technological or marketing advantage of the invention — why is it great? why are we excited?
5) drawings of the invention —handwritten or computer generated or whatever, just make them good.

Publication or Commercialization

Has your invention been published or described outside IDEA/Intel/HP or will it be soon? Y N Was an NDA used? Y N
Describe/Date:
Is your invention in any past, present, or future IDEA/Intel/HP product or planned to be? Y N
Describe/Date:
Has your invention been used in any IDEA/Intel/HP product that has been sold or offered for sale or will be soon? Y N
Describe/Date:

Supervisor's Approval

I have read this disclosure, approve of my inventors working on the invention, support them in investing the time and effort required to get a patent on the invention, and recommend that the honorarium be paid.

Name: Hans Mulder Signature: Date:

Principal Architect's Classification

(will be completed by Legal and the Principal Architect after submission)

EM Architectural? Y N Category: T X P Q Comments:

Additional Inventor(s)

Full Name: John Crawford Social Security No.:
Residence Address:
Mailing Address:
Hom Phone: Work Phone: Mailstop:
Employee No.: 10013000 Citizenship: Supervisor:
Employer: Intel or HP (circle) Business Group: Division/Lab:

Signature: Date:

Full Name: Greg Mathews Social Security No.:
Residence Address:
Mailing Address:
Home Phone: Work Phone: Mailstop:
Employee No.: 10048292 Citizenship: Supervisor:
Employer: Intel or HP (circle) Business Group: Division/Lab:

Signature: Date:

Full Name: Edward Grochowski Social Security No.:
Residence Address:
Mailing Address:
Home Phone: Work Phone: Mailstop:
Employee No.: 10045808 Citizenship: Supervisor:
Employer: Intel or HP (circle) Business Group: Division/Lab:

Signature: Date:

Full Name: Kosaraju, Chakravarthy Social Security No.: 230-49-9594
Residence Address: 1083 Rembrandt Dr, Sunnyvale, CA-94087
Mailing Address: 1083 Rembrandt Dr, Sunnyvale, CA-94087
Home Phone: 408-733-2950 Work Phone: 408-765-4812 Mailstop: SC12-502
Employee No.: 10056114 Citizenship: India Supervisor: Nimish Modi
Employer: Intel (circle) Business Group: MPG Division/Lab: IPD

Signature: Date:

Full Name: Social Security No.:
Residence Address:
Mailing Address:
Home Phone: Work Phone: Mailstop:
Employee No.: Citizenship: Supervisor:
Employer: Intel or HP (circle) Business Group: Division/Lab:

Signature: Date:

INTEL U.S. PATENT APPLICATION FILE REQUEST FORM

CONFIDENTIAL

COMPLETE AND RETURN FORM TO INTEL PATENT DATABASE GROUP WITHIN 2 DAYS Date Opened:

Return File To: K&K

TO BE FILED BY K&K

Matter #: P8686 Intel Grp Atty: LVN/INTEL Work Atty: K&K

TYPE OF INTEL PATENT APPLICATION FILE

*Patent: ☐ Utility ☐ Design ☐ Reissue ☐ Reexam

☐ Continuation (C) ☐ CIP (X) ☐ Divisional (D)

Title of File: METHODS FOR PROTECTING 1-HOT VECTOR TAGS IN A CACHE IN HIGH PERFORMANCE MICROPROCESSORS

INTEL DISCLOSURE AND FOREIGN FILING INFORMATION

*Disclosure number(s): 13106

*Product/Process:

Intel Committee: ARCHITECTURE Intel Group: MPG Intel Division: NONE

Foreign Filing: NEED Fast Track? NO

Countries:

Notes:

*INTEL ABSTRACT CODES (Check One or More)

__PROCESS (C1)
__N or P MOS (C1A)
__Equipment (C1B)
__CMOS (C1C)
__Contacts (C1D)
__Flash (C1E)
__GaAs and SOS (C1F)
__Circuit element (C1G)
__Isolation/Insulation (C1H)
__BiCMOS (C1I)
__Analysis/Testing (C1J)
__Etching/Planarization (C1K)
__Metal (C1L)
__Poly silicon (C1M)
__Passivation (C1N)
__Masking/Resist (C1O)
__Deposition (C1P)
__Implantation (C1Q)
__DRAMs (C2)
__Sense amp (C2A)
__SRAMs (C3)
__Sense amp (C3A)
__EPROMS (C4)
__P-channel (C4A)
__N-channel (C4B)
__Flash (C4C)
__EE (C4D)
__Sense amp (C4E)
__Solid-State disk (C4F)
__Flash Card (PCMCIA) (C4G)
__Multibit Cell (C4H)
__Redundancy (C4I)
__Blocking (C4J)
__Write Automation (C4K)
__Minicard (C4L)
__ Camera (C4M)
__ FMM (C4N)
__ Firmware Hub (FWH) (C4O)
__ Security (C4P)
__ Small Block (C4Q)
__ FDI (C4R)
__ Interface (C4S)
__ Connector (C4T)
__ Cell Phone (C4U)
__ Charge Pump (C4V)
__ Audio (C4W)
__ Microprocessor (C5)
__ Embedded (C5A)
__Buses Input/Output Devices (C5B)
__Protocol/CPU Interfacing (C5C)
__Adder/Multiplier Units (C5D)
__Numeric (C5E)
__Video/Graphics (C5F)
__Cache/memory Hierachy/ Memory/Virtual Memory (C5G)
__Memory Management/ Protection/Addressing (C5H)
__Instruction/Inst. Decoding/ Microcoding/Sequencing/ Microprogrammed Control (C5I)
__Pipeline/Parallelism (C5J)
__Clocking/Clock Generation/ Clock Multiplication (C5K)
__Addressing/Addressing Modes (C5L)
__Vector Processing (C5M)
__Registers/Files/Stacks (C5N)
__Multiprocessing/Dual (C5O)
__Initialization/Testing/ Debugging (C5P)
__Program/Program Control/ Interrupt/Status/Faults Exceptions (C5Q)
__RISC (C5R)
__Redundancy (C5S)
__SYSTEMS (C6)
__Bus (C6A)
__Supercomputers (parallel multiprocessors) (C6B)
__Compilers (C6C)
__Test Equipment (ICE) (C6D)
__BIOS (C6E)
__PCMCIA (thin removable functionality cards, i.e., memory, modem, network, etc.) (C6F)
__Magnetics (bubble memories) (C7)
__Buffers (C8)
__Packaging/Mounting/ Connector (C9)
__Logic (C10)
__Neural (C11)
__Miscellaneous (C12)
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(EXHIBIT A)

- **Title:**

  Methods for protecting 1-hot vector tags in high performance microprocessors

- **Filing data:**

  Inventors: Nhon Quach, John Crawford, Ed Grochowski, Greg Mathews, Chakravarthy Kosaraju

  use in Intel Products: Used in the Montecito processor

- **Context of Invention:**

  The context of invention relates to the design of a highly reliable high performance microprocessors.

  Naming convention and definition of terms: A cache that stores 1-hot vectors as tags is referred to in this disclosure as a 1-hot tag cache. Similarly, a cache that stores a 2-hot vectors as tags is referred to as a 2-hot tag cache. A 1-hot vector contains a 1 and a number of 0's in its bit pattern. A 2-hot vector contains 2 consecutive 1's and a number of 0's in its pattern. The right most bit in a 2-hot vector is called the primary bit and its left neighbor bit is called the aux bit.

  Background: Modern high-performance processors include on-chip memory buffers, called caches, to speed up memory accesses. These caches often consist of a tag array and a data array. The data array store the necessary data during the execution of the program. The tag array stores the physical (or virtual in some processor) addresses of the data. For reliability reasons, these stored tags are often parity protected for error detection. In even higher performance processor (such as the McKinley processor and future IA-64 processor), the tags are actually stored as 1-hot vectors derived during the TLB lookup for address translation. The protection of these 1-hot vectors presents a great challenge since the conventional parity bit scheme does not work. In this disclosure, we describe 2 methods to protect these 1-hot vectors: the first one uses a scheme called 1-hot plus valid bit and the second one uses a 2-hot vector scheme.

  The 1-hot plus valid bit scheme has the advantage that it is conceptually simple, but require a read modify write (a multi-cycle) operation on the valid bit. Area wise, it requires 1 additional word line for reading out the content of the 1 hot column. The 2-hot scheme is more complicated, but it does not require the multi-cycle operation. For certain implementation of the cell arrays, it does not require additional bit or word line.

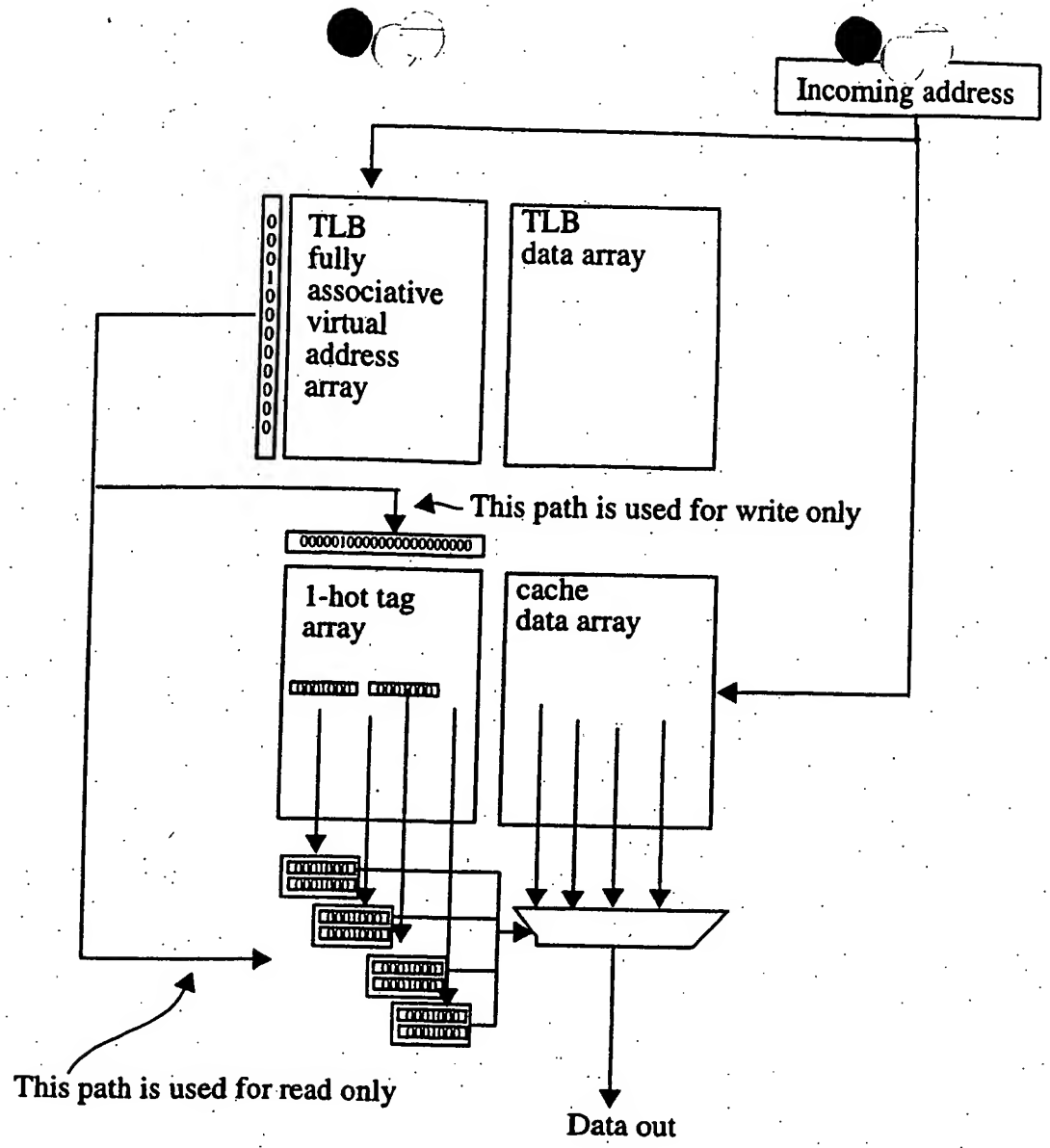
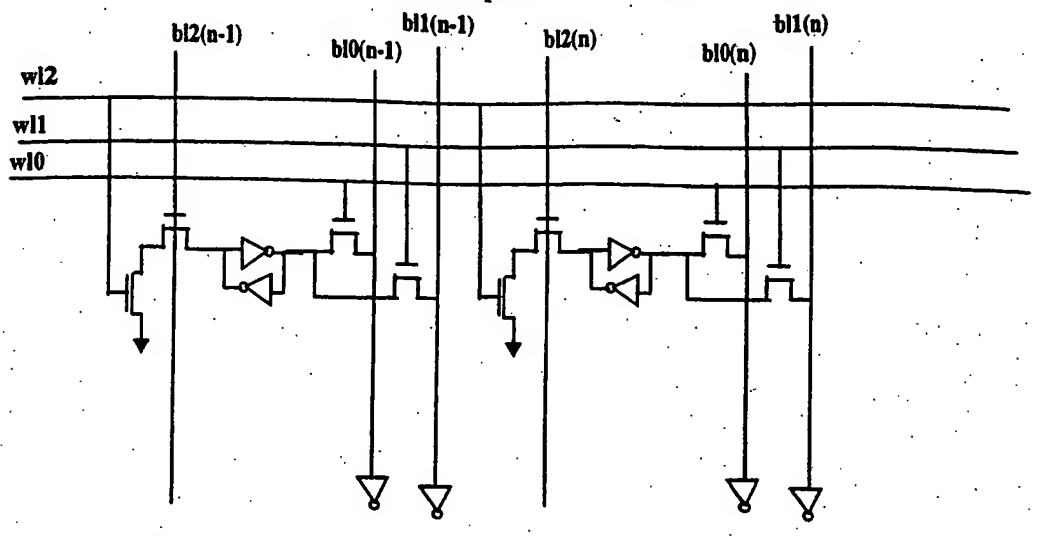


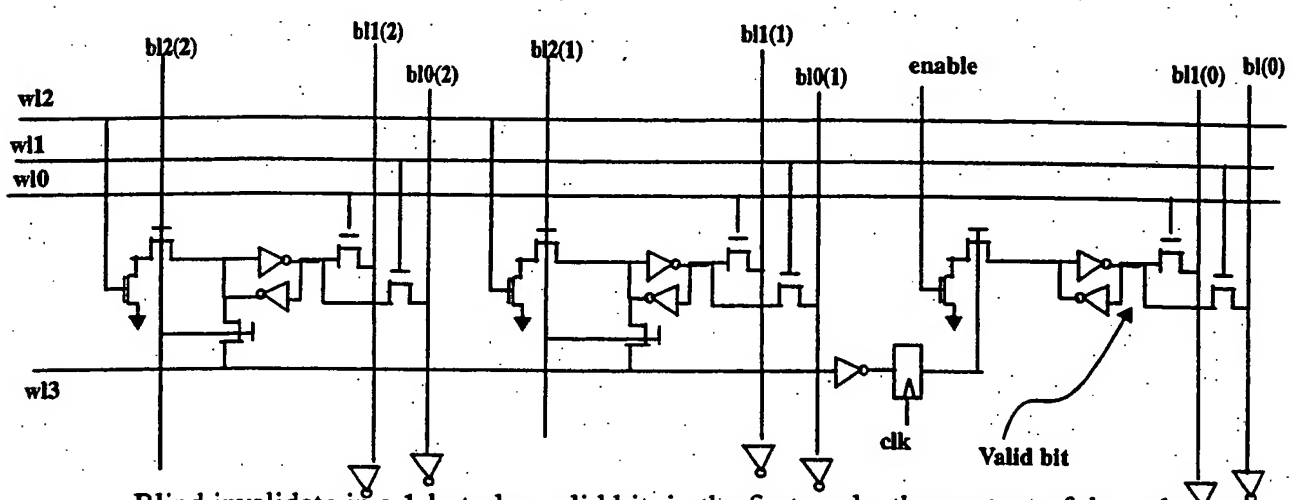
Figure 1 A 1-hot tag cache works the same way as a conventional cache, except that the tag is a 1-hot vector.

Background on the 1-hot tag: In the 1-hot tag cache, the 1-hot vector comes from the TLB lookup. When the virtual address of a cache access is presented to the TLB during the address translation, a 1-hot bit vector (of the size of the number of entry in the TLB) will indicate which entry in the TLB data array to read out the physical address. At the same time, this 1-hot vector will be used to compare the tags (also 1-hot) stored in the cache. A match will indicate the way to read out. On a fill, this 1-hot vector (also looked up from the TLB) will be written to the tag array. Since the 1-hot vector will only indicate the page a data belongs to, on a page miss and when a new page is brought in, all the 1-hot vectors in the cache that have the same bit pattern need to be invalidated. This is referred to as a blind invalidate operation. Figure 1 demonstrates the operation of a 1-hot tag cache.

1-Hot plus parity bit protection scheme: In this scheme, each 1-hot vector is appended 1 bit at the end, serving as the parity bit. Figure 2 shows how a typical tag cell is implemented and how it needs to be modified to implement the present invention.



Blind invalidate in a 1-hot tag cache. No interaction among the bits



Blind invalidate in a 1-hot plus valid bit: in the first cycle, the content of the column to be cleared is first read out and in the second clock, wl2 is asserted, both the 1-hot column and the valid bit will be cleared.

Figure 2 Comparison of a 1-hot and a 2-hot tag cache.

Operation of the 1-hot tag cell array: The operation of the 1-hot tag array is as follows:

- Read operation: wl0 or wl1 is asserted to read out the content of the bits in the array on the bit line bl0 or bl1.
- Write operation: a write operation is performed in 2 phases. On the first phase, one or both bit lines (bl0 and bl1) are grounded and one or both word lines (wl0 or wl1) are asserted. This forces all the bit in the selected row to be 1. On the second phase, wl2 and bl2 will be asserted. The data are indicated by the bl2 lines in an inverted form. That is, the locations where a 1 will be written will have a bl2 equal to 0. In this way, all bits are cleared to zero except that one that we want to store a 1.

Blind invalidate: all wl2 lines are asserted and the column to be cleared is again indicated by the bc signals in non-inverted form.

In the 1-hot plus valid bit scheme, 1 bit will be added to the 1-hot vector, serving as the valid bit. On a read, the valid bit will be accessed at the same time as the 1-hot vector. If the valid bit is set, the 1-hot vector is considered valid; otherwise, the 1-hot vector is considered invalid. The valid bit will be cleared on a blind invalidate as the 1-hot bit. The detailed operation of the 1-hot plus valid bit is described below.

(Note: the disadvantage of this scheme is that the added read port via wl3 will be very slow since wl0 and wl1 travel only 8 bits and wl3 must travel 32 bits. Also, the cells must now perform a read on both ports. The device sizes must be larger).

Operation of the 1-hot plus valid bit:

- Read operation: same as the 1-hot scheme. The valid bit is accessed as the same time as the 1-hot vector. A 1-hot vector that does not have the valid bit set is considered a soft error event and vectored into the error recovery firmware code. In this case, the FW will invalidate the entire cache.
- Write operation: same as the 1-hot scheme. The valid bit will be written at the same time as the 1-hot vector.
- Blind invalidate: This is performed in 2 cycles. In the first cycle, the 1-hot vector is indicated by the nbl2 bit lines. The word line wl2 is NOT asserted. The data in the column that is indicated by the 1-hot vector will be read out. In the second clock, the nbl2 lines continues to be asserted, the wl2 word lines will be turned on. This will clear both the 1-hot vector and the valid bit.

2-hot vector protection scheme: In this scheme, we convert the 1-hot vector to a 2 hot vector. This is done by local logic in the cache tag during the write operation of the 1-hot vector into the tag. During the read out, the 2-hot vector is automatically converted back to a 1-hot vector. In this way, the accesses of the cache works identically to the 1-hot tag cache. The conversion from 1-hot to 2-hot vector can be easily done. Figure 3 shows how a 2-hot tag cache works. It is similar to a 1-hot tag cache, but a 2-hot tag cache store 2-hot vectors, rather than 1-hot vectors.

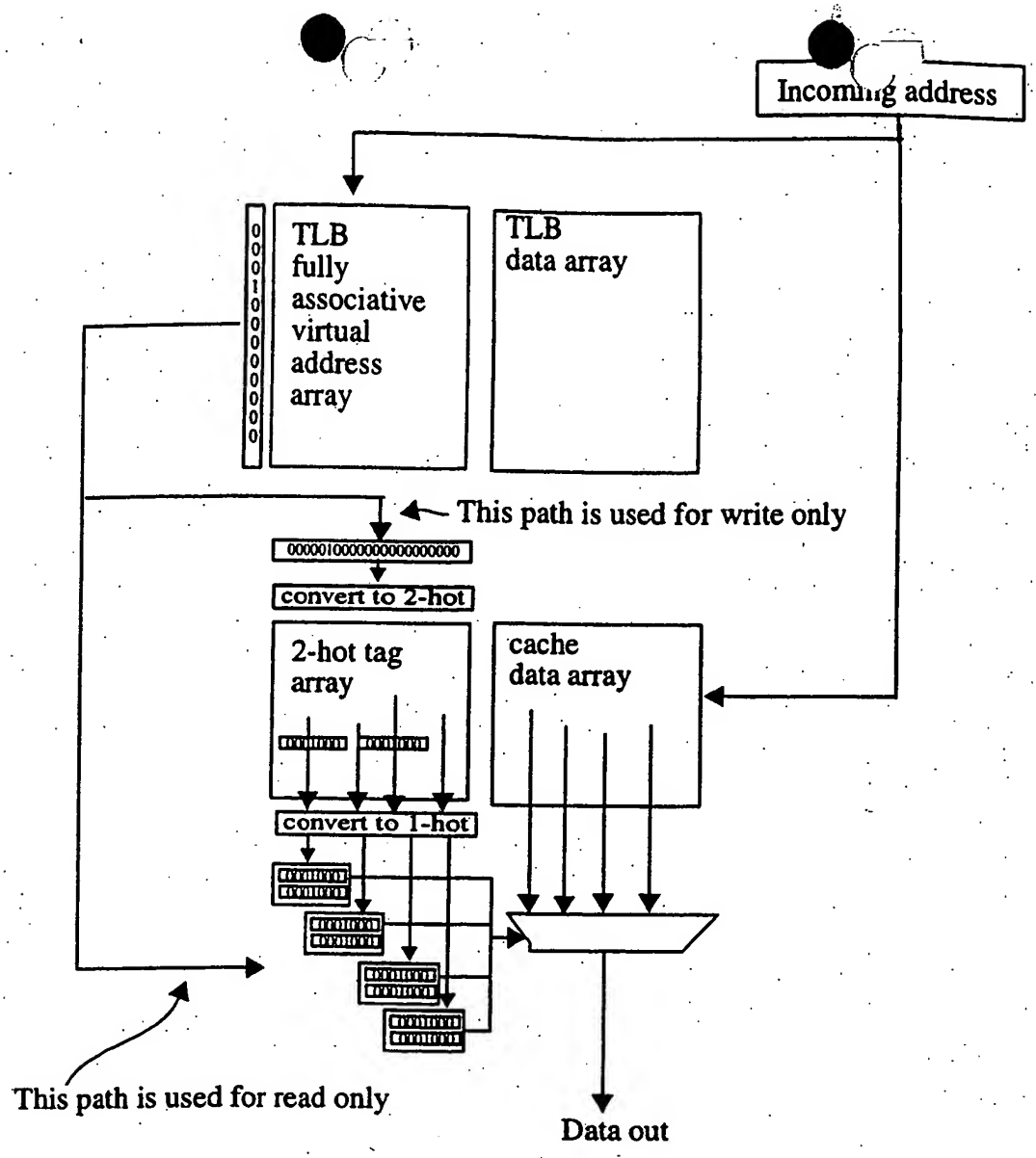
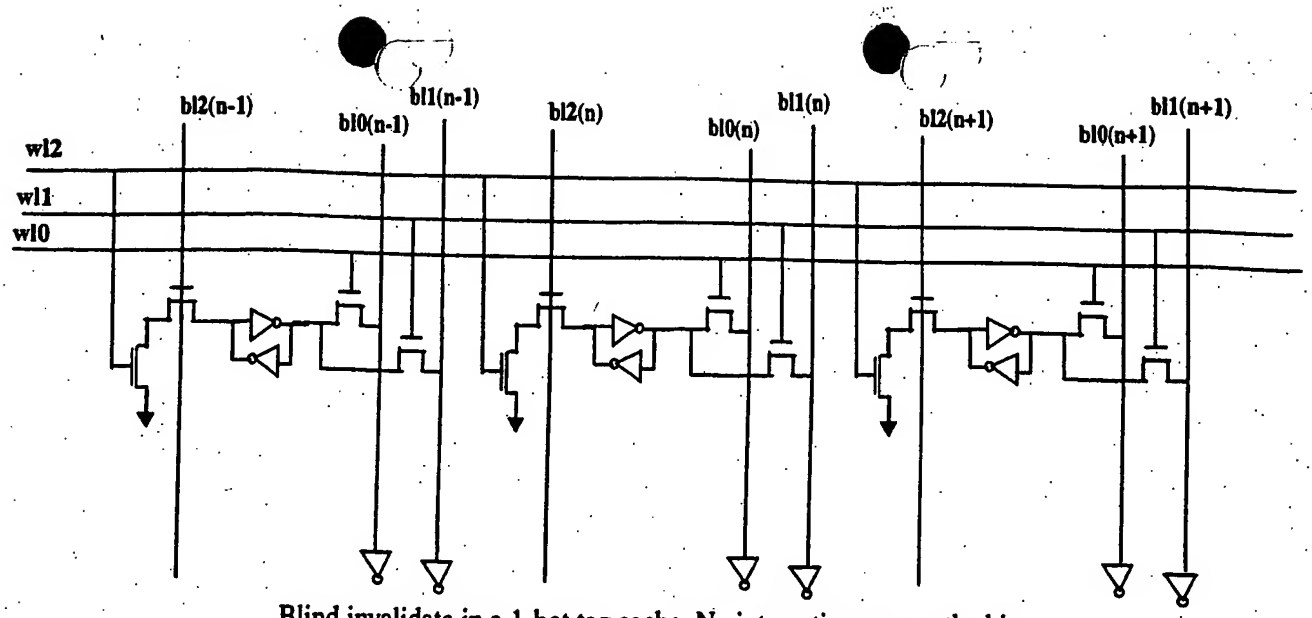
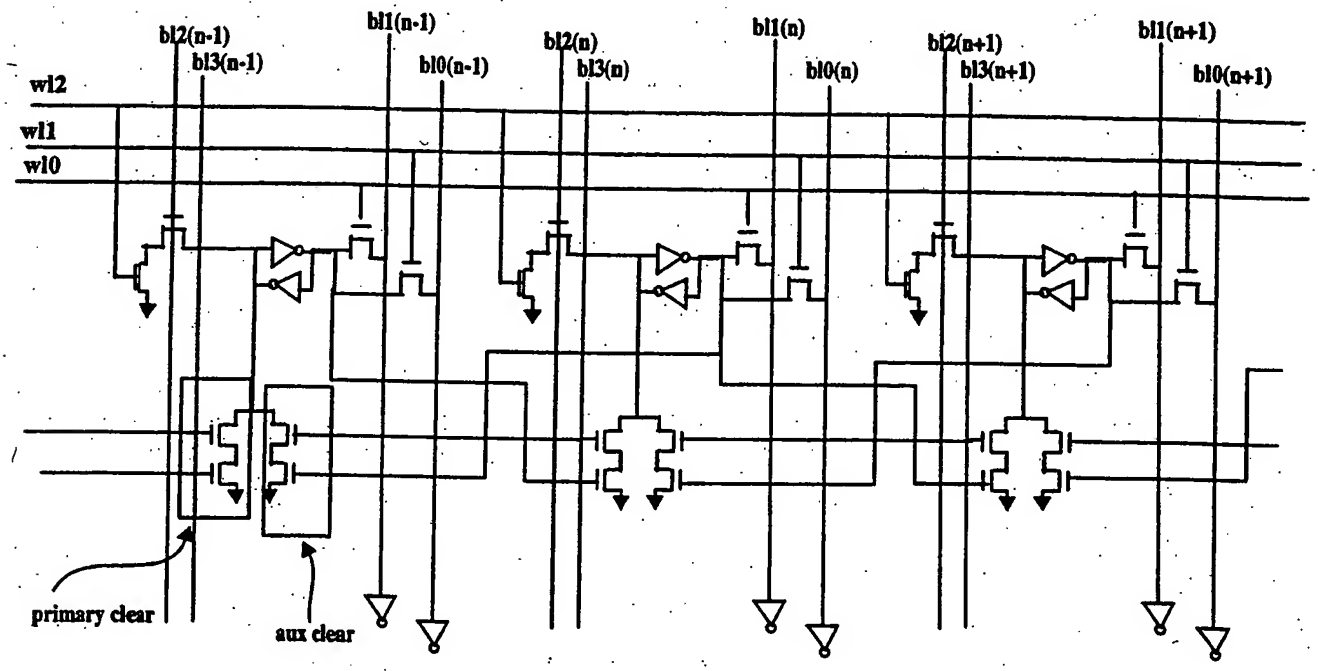


Figure 3 A 2-hot tag cache works the same way as a 1-hot cache, except that the tag is a 2-hot vector.



Blind invalidate in a 1-hot tag cache. No interaction among the bits

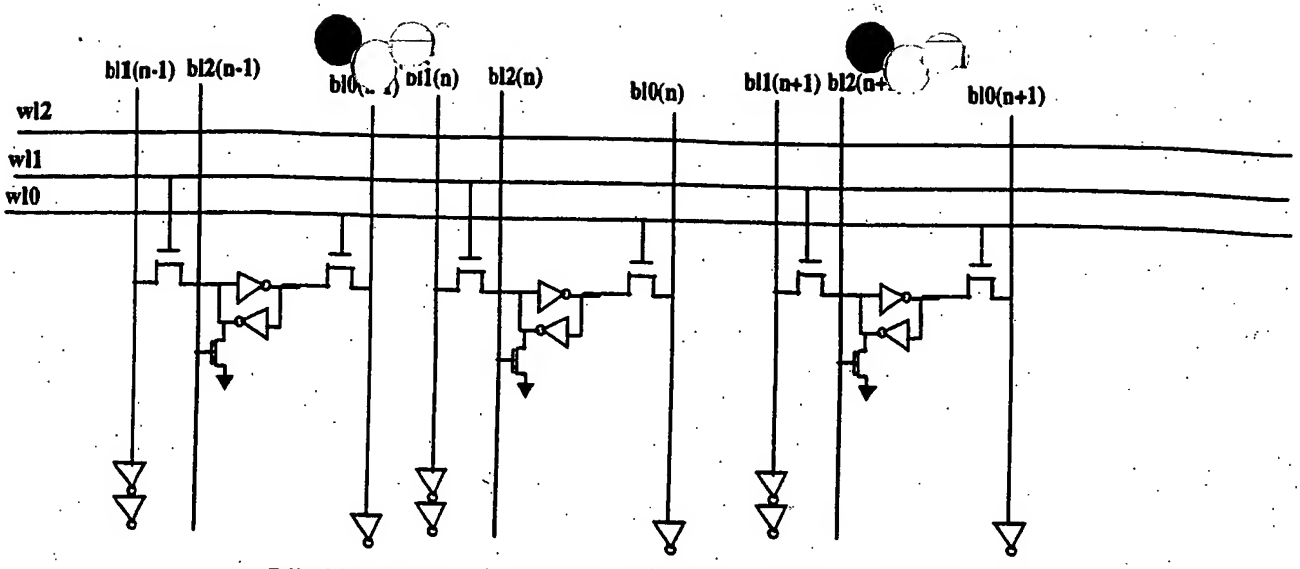


Blind invalidate in a 2-hot tag cache. A bit looks at its right neighbor blind clear signal (bc) and its left and right neighboring bits.

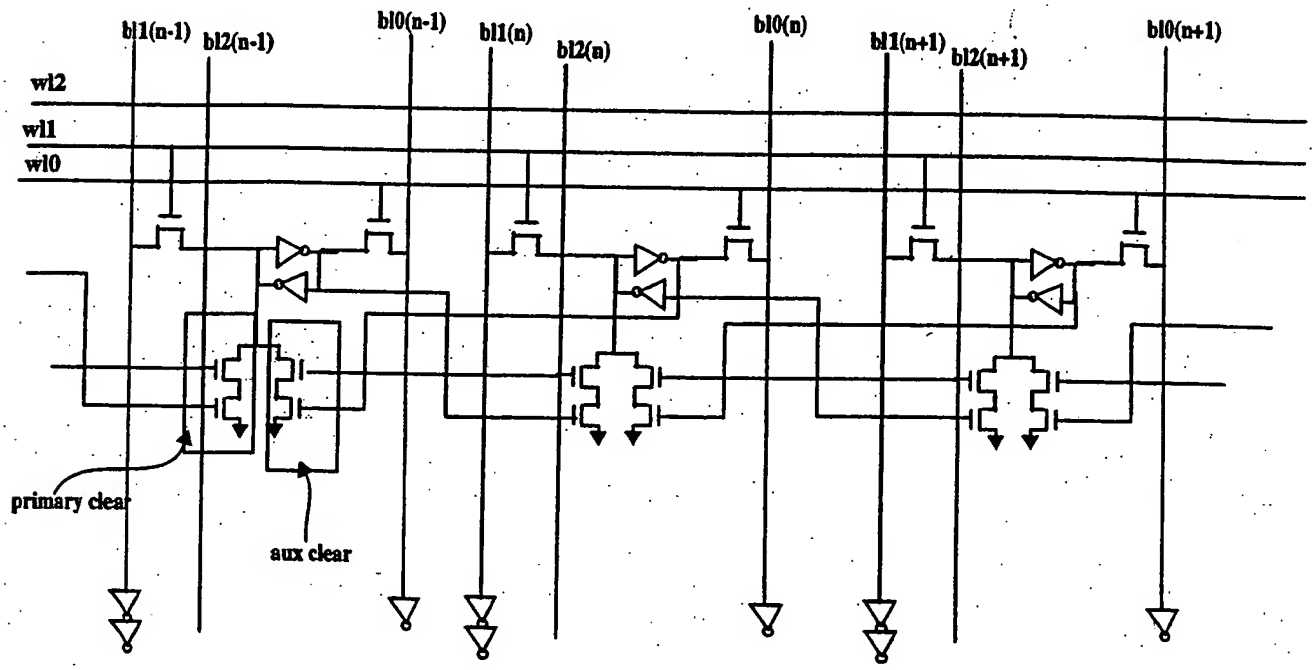
Figure 4 Comparison of a 1-hot and a 2-hot tag cache.

Operations of the 2-hot tag cache: The operation of the 2-hot tag array is again shown in Figure 4.

- Read operation: same as the 1-hot tag array case.
- Write operation: same as the 1-hot tag array case, except that the data will be a 2-hot vector, rather than a 1-hot vector.



Blind invalidate in a 1-hot tag cache. No interaction among the bits



Blind invalidate in a 2-hot tag cache. A bit looks at its right neighbor blind clear signal (bc) and its left and right neighboring bits.

Figure 4 Comparison of a 1-hot and a 2-hot tag arrays that use a differential write scheme

Generalization: the 2-hot scheme can be extended to a 3-hot vector to protect errors in 2 consecutive bits. Also, other bit patterns other than 2-hot may be used depending on the type of the errors one is trying to protect against.

The scheme described above minimizes global routing at the expense of local interconnect and transistors. Other schemes may use a multiple clock blind invalidation scheme by using a different signal for invalidating the aux bit.

- **Advantage:**

The advantage of both the 1-hot plus valid bit and the 2-hot scheme include: HW saving, higher speed, and simplicity. [redacted] t scheme can also be extended to [redacted] double bit errors.

- **Value to Intel:**

  This feature allows Intel to build more robust processors in the future. Specifically, this scheme will be used in the Montecito processor.

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ASSIGNOR:
CRAWFORD, JOHN DOC DATE: 03/29/2001

ASSIGNOR:
MATHEWS, GREG S. DOC DATE: 03/28/2001

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GROCHOWSKI, EDWARD DOC DATE: 03/30/2001

ASSIGNOR:
KOSARAJU, CHAKRAVARTHY DOC DATE: 03/28/2001

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Circuit and Method for Protecting 1-Hot and 2-Hot Vector Tags In A Cache In High Performance Microprocessors

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Nhon Quach

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Greg S. Mathews

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Edward Grochowski

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and in and to said application and all divisional, continuing, substitute, renewal, reissue, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements; and in and to all original and reissued patents that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application;

agree that said Assignee may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements; execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said Assignee, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally assist said Assignee, its successors, assigns, or representatives in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives; and

covenant with said Assignee, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Each Inventor: Please Sign and Date Below:

28 March —, 2001

C. S. Chakravarthy

Chakravarthy Kosaraju

Assignment Document Return Address:
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